French Norm

NF C 93-713

January 1989

Electronic components

Printed Circuit Boards

General prescriptions

French norm issued by order of the General Manager of AFNOR on 5th, december 1988 and effective 5th, January 1989.

Replaces the norm NF C 93-713 dated August 1974 and addition dated January 1978.

Corresponding : At present date, no international norm exist on this subject.

Analysis : This norm concerns printed circuit boards with how to express general characteristics and particular characteristics.

Description : Electronic components, printed circuit boards, technical files, class, dimensions, delivery controls, repairs.

Modifications : Compared to last edition, this norm does not include quality insurance matters. It gives additional information about dimensions to be taken care about , depending on the class of the board.

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1. GENERALITIES

1.1. Field of application

The present norm applies to single side, double sided with plated holes and multilayer printed circuit boards made on phenol or epoxy resins with fibre glass or reinforced celluloid paper, made with addition or subtraction method and which conductive areas are made of copper, with and without solder mask and/or legend.

1.2. Object

This norm has to:
- Define the product while fixing general characteristics and the way to express the specific characteristics,
- Recommend the conditions to receive and accept the batches delivered.

It does not tell about the conditions of homologation nor the quality norms.

1.3. Documents for reference

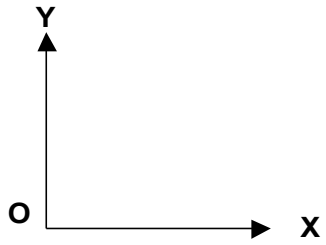
- NFC93-702: test methods on PCB
- NFC93-715: PCB: characteristics and control of production films
- NFC93-716: PCB: control of continuity and lack of short cuts with automatic tools: general descriptions
- NFC93-721: Repairs of PCB: General condition
- NFC93-750: PCB: base material test methods
- NFC93-751: PCB base material general prescriptions
- UTEC93-751: PCB base material list of particular specifications
- UTEC93-703: Conception and use of PCB guidance
- UTEC93-723: Usage and repair of PCB guidance
- CEI97, 194 and 326

These norms and CEI publications are available at UTE.

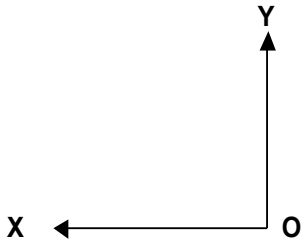
1.4. Definitions.

1.4.1.Reference axis of a board; normal way of reading.

Two orthogonal axis OX and OY are seen in the normal way of reading; OY results from 90° counter clockwise turn of OX.



As seen from reference side.



As seen from opposite side.

- The reference side of a board is the side that is shown in the normal reading way. Its is numbered 1.

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- Reference axes of a board are used to define all the coordinates, the position of outside elements, the routing and scoring, the holes centres, the centres, axes and routes of printings and other elements, with or without grid as per CEI 97 publishing.

NB: documents of printed via, selective coatings, printings and all other constitutive elements (mass-lam, thermal drain, etc) use similar reference axes which position is defined relatively to the axes of the board.

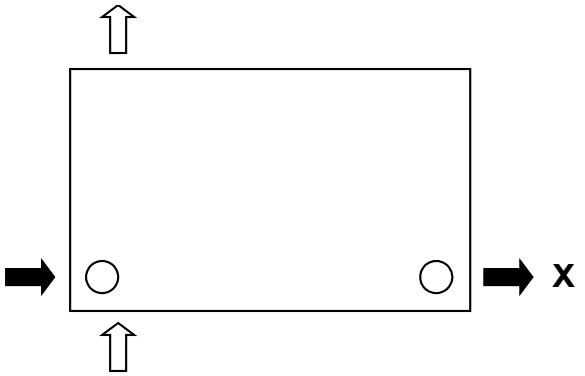
1.4.2.Indexation system of a board

This system materializes the reference axes of a board.
The indexation system of a printed circuit board is made of:

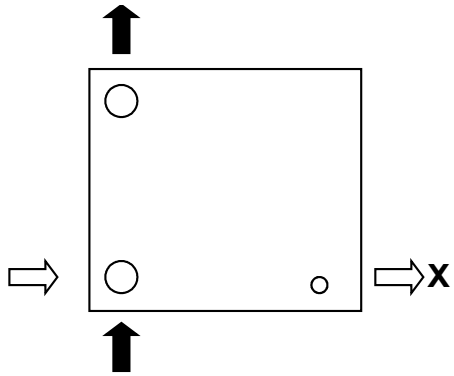
- Either two non-plated holes (drilled with the other holes and protected from plating with tenting, or drilled again based on optical targets)
- Or with two datum (marks on copper) for optical targets.
- And one easy recognizable indication of the reference side of the board.

The origin of the reference axes is in the centre of one hole or one datum, and one of the axes passes through the centre of the second hole, as indicated on the drawing of the reference side in the technical file, and as per following principle:

- OX axis is indicated with "X"
- Axis defined with the two indexation holes is indicated with a black arrow
- The second axis, perpendicular, is indicated with a white filled arrow
- If the reference side is materialized with a third hole situated on the second axis, this hole must be clearly different from the two others in its diameter or in its distance from the origin hole.



Example 1



Example 2

NB: these principles can be followed partially if the result will not lead to confusion or loss of precision. But extra care must be taken for multilayer, big size, SMT and automated insertion boards.

Index system is used to:

- Control and verify the position of centres, axes, routing and printings on the board
- Position the reference axes of the board with an external system using them (example : automated insertion machine, surface mounting machine, etc)

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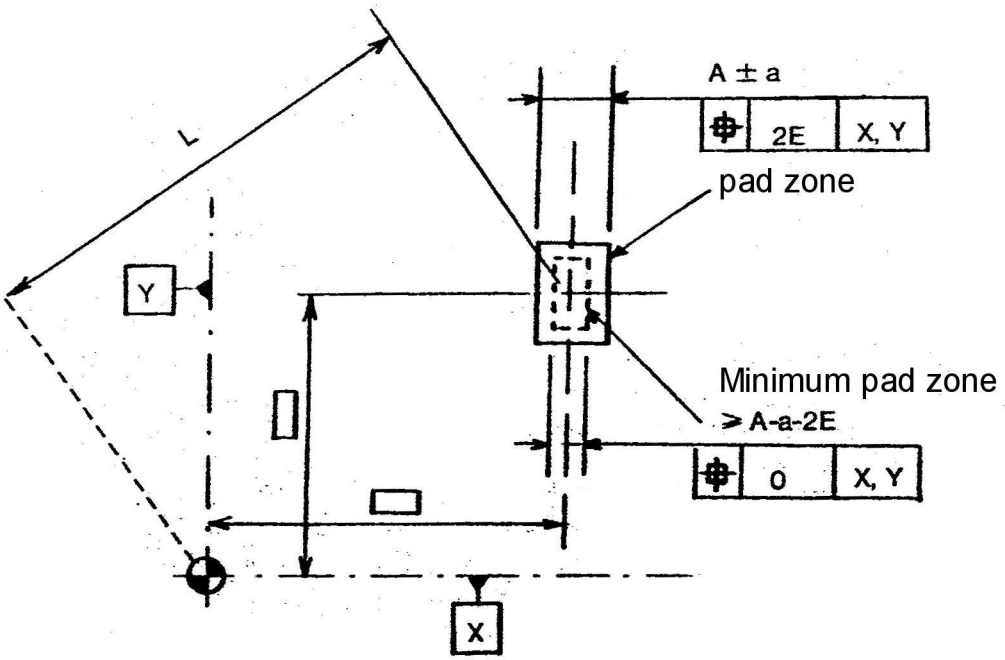
1.4.3.Minimum pad size for surface mounted components (SMC or SMD)

Pad = area made of conductive material on the external side of a board and used to connect one component end.
Minimum receiving area = part of a pad, centred on its nominal position and of a minimum size as per dimensions and position tolerances, where conductive printing can receive the connection and in which the component end must be located.



NB:
a: pad width tolerance as per class
E: error on centre position, as per class and L data (distance from the centre of the pad to the designed centre for placement)

1.4.4.Computer data

Information recorded on any support and that can be accessed directly or via electronic transmission (email, modem…).

2. TECHNICAL FILES

2.1. Content

The technical file consists of whole documents (written, drawings and data files) which indicate the general and specific characteristics of a printed circuit board. It contents the present norm and the documents which it refers to, and the documents submitted to the manufacturer:
- The technical file (§2.2);
- The drawings and complementary documents for mechanical description: centre holes film, or drilling program, drawings and programs for routing (§2.4);
- the definition documents of the printings, selective coatings, legends, etc (drawings, films or computer files) (§2.5);

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- Marking and wrapping instructions (§2.6);
- Customer's specific requirements (§2.7).

NB: When setting up the technical file, the customer will consult the manufacturer to set-up the elements which are linked to the manufacturer technology; therefore, this file can first be set as an intention before being completed to reflect the contractual specification; the file must be complete, settled in all details and identified by its date or revision number on time of delivery.

2.2. Technical file

The technical file is the document done by the customer by filling a copy of the Technical File.
In Appendix A is the technical file for rigid pcb's.
All specifications that are not on the technical file must be indicated in texts, drawings, films or computer files which references are indicated in and are part of the technical file.

2.3. Additional drawings and documents for mechanical description.

Unless otherwise stated, the drawing is a sketching of the reference side of the board. Usually it does not show the PCB pads or lines.

- It shows the boards reference axis and indicate their location relatively to the locating system – reference holes or copper target for optical aiming – and their characteristics (holes diameter, picture and size of the optical targets). If the shapes or dimensions of the board outlines cannot be used to identify the reference side, the locating system is indicated on the drawing with a hole or sketch, separately from those defining the axis directions (see chapter 1.4.2).
- It shows the outline and the inner routing of the boar and sets the dimensions; for more clarity, these dimensions can be indicated as related to a routing plan, which is a separate document or with a computer data file (automatic routing program).
- It shows the drillings and defines:
  * The diameters, either clearly (for holes drilled afterwards) or by coded indications with explanations on the same document as the one which shows the location of the holes.
  * the location, either by using a grid (the x/y locations of the centre of the holes are then indicated in multiples of the grid steps) or relatively to the lines dry film of the recto side or with a "holes centres film", or with their position (especially for drillings afterwards) or by quoting the computer data file of the automatic routing program.

  NB: Avoid redundant data; for the remaining ones, (for example drawing and data file) a hierarchy must be set. In principle, the drawing is the reference. Usually a first article can insure there are no mistakes.

2.4. Document setting the Films list.

The models of lines and pads, of solder masks if need be, of selective metallization and of markings are usually made of films or computer data files for automatic imaging systems. In all cases the documents holds one reference and the reference of the PCB. The tolerance of this document must be relative to the tolerance needed on the PCB (see

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chapter 3.3) and must satisfy to the specifications (NF C 93-715 for the films) or to the contract between the customer and the factory.

2.5. Electric Test (Etest) program.

The electric test is a series of unit test to check continuity and lack of shorts as per NF C 93-716. It is needed for control before delivery and is designed by the manufacturer and approved by the customer and is made of the automatic test bench program. If this program or the board characteristics does not allow a full control by this mean, then a partial test is set indicating the pairs of points in which continuity or shorts must be tested.

NB: Marks done by test pins on the SMC land zones must be avoided. If possible test points must be located on a test pad.

2.6. Marking and wrapping indications.

Marking instructions indicates the content and the location of the marking to be put on the PCB and on the wrappings.
Wrapping must be done so to protect the cards in normal transportation conditions (especially wear and tear, fall down or rain). The number of PCB per carton is limited by the weight of the carton which must follow the rules of the transportation company and of the customer.
If the wrapping must satisfy to special storage conditions (for example long time, high humidity or special temperature) it must be contracted between the manufacturer and the customer.
UTE C 93-703 can be used as a guide for wrapping information.

2.7. Customer special requirements.

PCB special requirements indicated in the technical file, in the complements or derogating to the present norm are clearly indicated in the reverse side of the technical side and can refer to other customer documents.

3. DIMENSIONS

These characteristics are indicated in the PCB technical file.
This norm indicates the normalized values:
- for certain nominal characteristics for standardization purpose;
- for certain tolerances to simplify indications and as guidance to special contractual cases if need be.

For each value, the proposed tolerances can correspond to:
- different manufacturing technologies and costs
- different manufacturing difficulties due to certain PCB constraints (sizes, thickness of copper layers, number of layers etc);
- different customer needs linked to the components or the technologies used (manual or automatic).

These normalised values were established in partnership between the involved parties when writing this edition in 1988. They will need to be revised periodically to integrate the technological evolutions. Because some are due to common causes, they have been put together and globally treated and grouped under the indication of “class” (see chapter 3.3).

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3.1. Dimensions of a board

This norm does not establish nominal sizes; but it sets in table 1 one or several normalised tolerances. If the PCB technical file does not indicate a value, the applicable tolerance to use is the largest one.

Table 1

Characteristics	Tolerances				
Length and width (mm)	+/-2	+/-1	+/-0.5	+/-0.2	0(*)/-0.3
Thickness (copper to copper) (%)	+/-10	Double side (for multilayer boards see UTE C 93-751)			
Board sides angle (mm/m)	+/-2.5	+/-1.5			
Twist and wrap – test described in chapter 6.5	+/-1.5	+/-1	+/-0.8	+/-0.5	
(*) Use NF C 20-152 (HD493-3) "Dimensions of mechanical structures of 19 inch series – 3rd section"					

NB: for inserted connectors, a tolerance of +/-5% on PCB thickness can be necessary (see NF C 93-025)

3.2. Diameters and tolerances of holes.

3.2.1.Non plated holes for PCB less than 3.2mm thickness

Table 2

Nominal diameter (D) (mm)	Tolerances
From 0.80 to 1.35	+/-0.05 for D less or equal to 1.00
per 0.05 mm step	+/-0.10 for D above1.00

NB: Punched holes usually have a cone shape on one side.

3.2.2.Non plated holes for PCB less than 3.2mm thickness

Table 3

Nominal diameter Finished hole internal diameter (mm)	Tolerances (mm)	Metal thickness (um)
From 0.70 to 2.00 > 2.00 per 0.05 mm step	+0.10 / -0.05 +0.15 / -0.10	} ≥25 µm

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NB: Holes for inserted connectors are defined in NF C 93-025.

3.2.3.Plated holes for connection (via holes).

Table 4

Nominal diameters of drilled holes (see picture) (mm)	PCB thickness E (mm)	Metal thickness (um)
≥ 1	3.2 ≤ E < 6.4	≥ 25 µm
≥ 0.80	2.4 ≤ E < 3.2	
≥ 0.50	1.6 ≤ E < 2.4	
≥ 0.30	0.8 ≤ E 1.6	

NB: There is no tolerance for inner diameter of finished hole.

3.2.4.Holes with mechanical function, drilled afterwards.

Diameter as per drawing; tolerance +/-0.05mm.
Holes diameters must not be less than one fourth of the board thickness.

3.2.5.Indexation holes (see chapter 1.4.2)

Non plated holes drilled at the same time as the platted holes but protected from plating by tenting, or drilled after with optical aiming (for example punched boards).

Table 5

Nominal diameter (mm)	**Tolerance (mm)**
Being studied Maximum 4.00	+0.05 0
Distance between hole edge and copper area	≥ 1

3.3. Class of a PCB.

3.3.1.The class indicates :

- the density of connections per side (layer) as per criteria relative to dimensions and position of the copper area and the holes;
- the board / components interface as per criteria relative to tolerances of dimensions and components holes positions or SMC pads.

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3.3.2. The class is designated by a code made of:

- one digit from 1 to 6 which indicates the "density"
- one letter A to C which is relative to "interface".

3.3.3. For a card to be submitted to a class requirements, the following conditions must be verified :

- the design dimensions comply with conditions of a class requirement as per table 6a and annex B;
- the films and the drilling data comply to class conditions as per table 6b;
- the computer files provided must allow at least the same precision;
- the base material is compatible with position tolerances (chapter 3.5) of the corresponding class as per table 6a and 6b.

3.3.4. Class 1A to 6C are in a rising complexity; they apply to PCB of this norm in the limits of the manufacturer know-how: these limits refer to the number of layers or the size of the board, but also on other parameters. They correspond to the possibility to comply with all requirements of the board at the same time. Therefore each particular case must be approved between customers and manufacturer.

The A class correspond to the tolerances that normally applies to all cards referring to this norm. The B and C class only applies after agreement between the customer and the manufacturer in each particular case, because to satisfy the requirements depends from the PCB parameters and from the technology (for example, SNPB plating can generate more board twist and wrap or more mis-registration between solder mask and pads). See table 6a and 6b.
The class 4 to 6 are normally not used for cards made with silk screens.

3.3.5. If a side (or a layer) is not regular in density, the highest class applies to this layer (or side). Generally speaking, the class of a board is the class of its highest layer (or side) class.
The "interface" character refers globally to the holes and pads of the two sides.

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Table 6a

Criteria of a class Design values	Class 1-	2-	3-	4-	5-	6-(2)
Total copper thickness on sides (µm) Maximum values for inner layers	105 105	105 105	105 70	70 35	50 35	35 17.5
Minimum line width (mm)	0.80	0.50	0.31	0.21	0.15	0.12
Minimum space (mm) : - between lines or - between line and pad or - between pads :	0.68	0.50	0.31	0.21	0.15	0.12
Minimum difference (in mm) between diameter (1) : - of a component hole and the finished hole : - non plated through holes (NPTH) - plated through holes (PTH) - of a via pad on one side and the drilled hole	 1.57 1.19	 1.13 0.78	 0.90 0.60 0.45	 0.49 0.34	 0.39 0.24	 0.35 0.20
(1) These values applies to single side and double side PCB (NPTH only) . For multilayer boards see annex B. (2) Class 6 is for reference only.						

For a PCB with solder mask :

Minimum distance between solder mask edges and lines or pads (mm)	0.34	0.25	0.15	0.10	0.07	0.06
Minimum solder mask line width (mm)	0.80	0.50	0.31	0.21	0.15	0.12

Table 6b

Criteria of a class Limit values measured on film	Class 1-	2-	3-	4-	5-	6-(1)
Minimum line width (mm)	0.70	0.45	0.28	0.19	0.13	0.09
Minimum space (mm) : - between lines or - between line and pad or - between pads :	0.60	0.45	0.28	0.19	0.13	0.09
Difference between supposed position from the centre of a pad or window (centre is determined from the outline of the area)	0.20	0.10	0.05	0.04	0.03	0.03
Difference between pad or window centres that should be aligned (films alignments)	0.15	0.10	0.07	0.05	0.04	0.04
(1) Class 6 is for reference only.						

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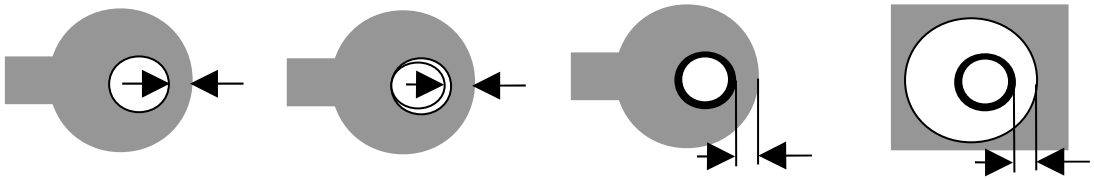
3.4. Dimensions of the copper areas.

The dimensions of the copper areas are defined by (see chapter 2.4):
- either by a drawing or a film which limits are set in table 6b.
- or by numerical values on a drawing with dimensions or in a computer data file (for automatic imaging software)

Table 7 summaries the tolerances that apply to the measured dimensions depending on the class.

Table 7

Class requirements : Measures on the board (mm)	**Class**					
	1-	**2-**	**3-**	**4-**	**5-**	**6-(1)**
Line and space width Tolerance relative to design data and given documents +/-	0.24	0.15	0.08	0.06	0.05	0.04
Minimum distance between pad edge and hole : Picture 1 NPTH Picture 2 PTH for component on external layers Picture 3 PTH for component on inner layers, via on external and inner layers	0.20 0.05	0.20 0.05	0.20 0.05 0.02	0.05 0.02	0.05 0.02	0.05 0.02
Picture 4 Inner layers minimum distance between the edge of a copper area and the edge of a non connected PTH (see note1)			0.33	0.23	0.17	0.14
 Picture 1 Picture 2 Picture 3 Picture 4						
(1) Class 6 is for reference only.						

Notes:

1) Annex C indicates a way to measure internal layers mis-registration.
2) When pads size or shape is smaller than the smallest round pad of the relevant class, the minimum annular ring (picture 2) is equal to: 0.05mm + ((round shaped smallest pad - selected smallest pad) / 2.

Example class 4; hole diam. 0.8mm

- round shaped pad minimum 1.29mm : minimum annular ring 0.05mm
- round shaped pad diam. 1.38mm : minimum annular ring 0.095mm
- square shaped pad 1.27mm : minimum annular ring 0.04mm i.e. 0.05 + (1.29 – 1.27)/2

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3.5. Position tolerances.

The position tolerance is the difference between:
- centre of a hole or centre of a pad calculated from its outline

and
- the nominal position of this centre, defined in the indexing system or in the drawing or the drilling data file or from films.

The position tolerance from one hole or pad to another is measured using the last one to generate auxiliary axis parallel to the reference axis of the board.

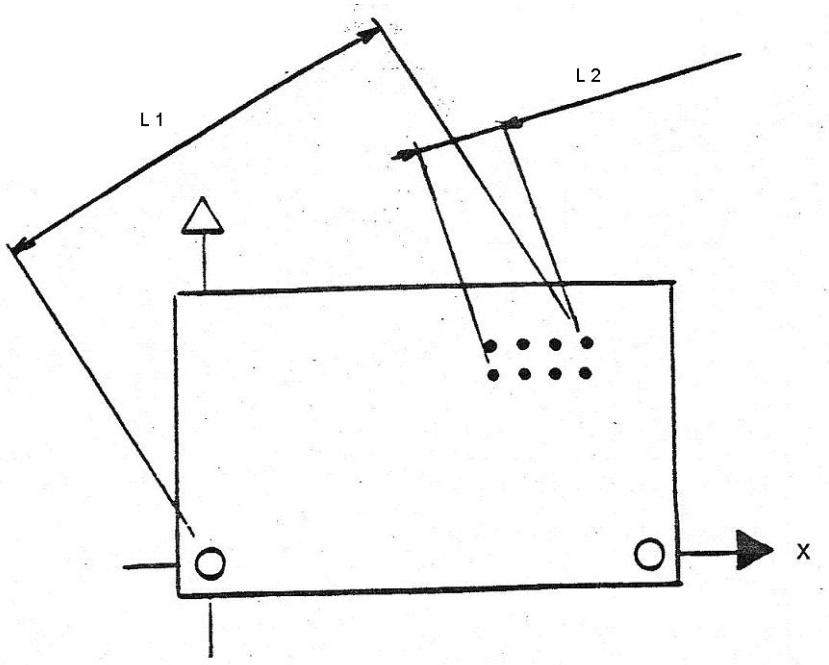
For *manual insertion*, the tolerance is measured between holes or pad centres of a same component (L1). (The drawing must indicate the components which have a distance between extreme pins of more than 100mm).

For *automatic insertion*, the tolerance is measured between holes or pad centres relative to the reference hole or the fiducial mark used for the automated machine (L2).

For components bearing centring pins, the tolerances are:
- centre errors measured between components pads and holes for centring pins
- and for automated insertion, centre errors measured between centring pins

Positions tolerances indicated in table 8a and 8b are relative to the class and depending on the distance L from one centre to the origin which is chose as the reference.

The largest value of L (L max) is indicated in the specification file.



Position tolerance:
L1 for automatic insertion
L2 for manual insertion

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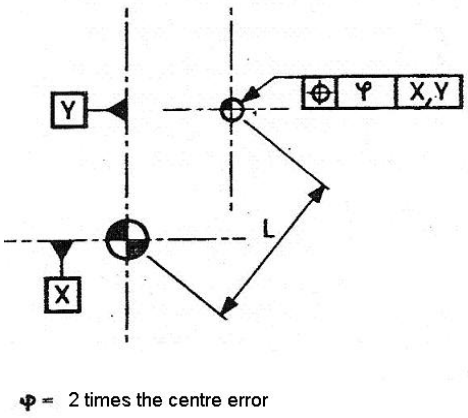
Table 8a

Holes tolerances relative to the indexing system.

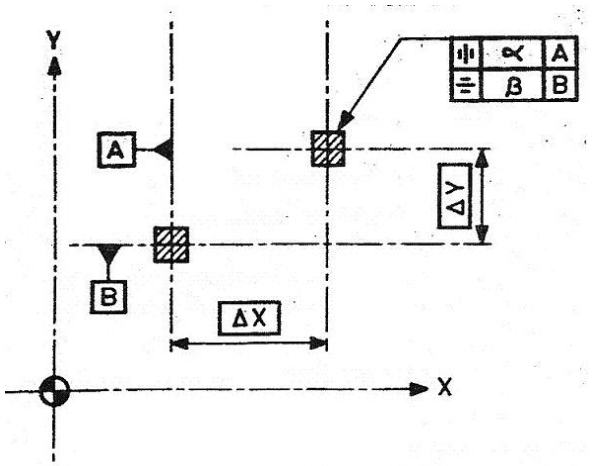


Tolerance φ	Class		
	-A	-B	-C
0.10		L ≤ 137	L ≤ 200
0.15	L ≤ 270	137 < L ≤ 410	200 < L ≤ 600
0.20	270 < L ≤ 390	410 < L ≤ 600	
0.25	390 < L ≤ 500		
0.30	500 < L ≤ 600		
0.35	600 < L ≤ 750		
0.40	750 < L ≤ 850		

All values in mm.

Table 8b

Position tolerances for SMC pads.



α, β = 2 times the centring error

Example Class 4-B : ΔX=100 Tolerance α=0.08

ΔX and ΔY ≤ (mm)			Tolerance α, β (mm)			
As per class			As per class			
-A	-B	-C	3-	4-	5-	6-
20	30	40	0.08	0.06	0.05	0.04
50	80	120	0.09	0.07	0.06	0.05
90	140	200	0.10	0.08	0.07	0.06
140	220	320	0.12	0.10	0.09	0.08
200	320	460	0.14	0.13	0.13	0.12
260	420	600	0.17	0.16	0.16	0.16
380	600		0.23	0.23	0.22	0.22
460			0.26	0.26	0.26	0.26
600			0.34	0.34	0.34	0.34

Class 6 is for reference only.

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3.6. Solder Mask dimensions.

The thickness of the solder mask is depending on the product and the process used by the PCB manufacturer. The requirements depends from the process (see annex D).

The dimensions and positioning of the solder mask are defined as the copper areas (see Chapter 2.4, 3.3 and table 6a and 6b).

Whatever class is considered, the requirements are :
- no solder mask on components pads
- solder mask must be present on all copper areas mentioned on the drawings
- no solder mask on areas mentioned so on drawings

Nevertheless, if the solder mask application process is not compatible with limits set by class, (for example silk screen solder mask for class 3 PCB) then the light requirement of annex E can be used after agreement between the manufacturer and the customer.

4. ELECTRICAL CARACTERISICS

Unless otherwise stated in the "special customer requirement" document, the following characteristics apply for all boards, and the way to apply them are described in the technical file.

4.1. Continuity and lack of shorts.

As per NFC93-716 or equivalent; the technical file must indicate the special needs as per chapter 2.

4.2. Testing voltage.

As per NFC93-050 chapter 2, with 100 volts DC (sudden application) applied to whatever pair of lines or pads which are not linked by copper.
Customer special requirements can designate one or several pairs of test points and another testing voltage.

4.3. Isolation voltage.

Measured at 100 V between any pair of conductors (lines or pads) which are not linked together. Isolation is measured after 1 minute.
Minimum requirement : board can be used if $R \geq 10^4$ MΩ under normal atmospheric conditions.
Additional requirement from customer can focus on one or several conductive parts and higher minimum resistance.

5. BASIC CARACTERISTICS

These characteristics comes from manufacturing process and from material used during the production. Most of them can only be precisely defined with sophisticated testing equipment. It is not always possible or necessary to test every batch before delivery.

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To verify the characteristics after agreement between manufacturer and customer, some test coupons are associated with the boards or with the batches :

- testing coupons can be removable parts of each board, associated with the board during production and set to tests the boards
- testing coupons can be independent and manufactured at same time and with same processes in order to test the manufacturing processes

These characteristics and way to test them are not part of this Norm. This Norm only indicates which norm must apply on the technical data sheet : NFC93-702 (or CEI326) which concerns about Quality and customer's specification.

Delivery of PCB according to this Norm implies that the processes and the materials used to manufacture them can allow to achieve basic requirement of the specification.

6. QUICK TESTS FOR ACCEPTING DELIVERIES

These tests are not to define basic characteristics, but only to check rapidly at low cost that the delivered boards do not have important defaults from manufacturing errors or accidents.

6.1. Solder ability test.

In wave soldering, in real conditions similar to user conditions , visual examination.
If solder ability defaults appears, full NFC93-702 (chapter 8.2) test must be done.

6.2. Ionic contamination test.

If required and agreed. If tests as per chapter 4.3 is found defective, the full NFC93-702 (chapter 6.4) test must be done.

6.3. Tear off test of pads on single sided PCB with no plated holes.

As per NFC93-702 test 11a (chapter 7.2.1).

6.4. tape adhesion test.

As per NFC93-702 test 13a. This test is intended for all metallization finish (chapter 7.2.1) and is used to verify tracks and small pads adhesion as well as solder mask and silk screen marking adhesion.

6.5. Wear and twist.

The board will slip on a sloped plane area and must pass through a levelled gate. The gate heights will be a % of diagonal of the board.

6.6. Inner layers misalignment.

This test will be conducted on the test coupon (see annex C).

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7. REPAIRS

Norms NFC93-721 and UTEC93-723 or any amendment of these Norms can applies if agreed between the customer and the factory.

8. DELIVERY ACCEPTATION

8.1. The boards must be delivered according to agreements between the factory and the customer, in homogeneous batches.
PCB of homogeneous batch are made :
- from same batch of raw material (laminate, copper etc) from one same and homogenous batch
- using same films or same software data in automated systems.
- on the same equipments and using same automation
- in the same chemical batches without changing the parameters
- using the same press (for multilayer pcb) and with same settings

8.2. according to customer's demand, the factory must deliver a CERTIFICATE OF CONFORMANCE" to this Norm and to the specification.

8.3. The delivery checks done by the customer on each batch after finishing, and that can be repeated by the factory, are sets between themselves. This check list is defined by the customer specification and the technical data sheet.
As per agreement, one part of these checking can be omitted or done in the manufacturer's premises using the same check list or harder check lists. In this case a checking report is attached with every batch delivery.
Reference to this Norm implies that the testing program include the following checks:
- conformity to the PCB reference and to the marking
- conformity to the dimensions, according to chapter 3
- electrical conformity according to chapter 4
- quick tests according to chapter 6
- outlook control as per appendix F
- conformity of packing and of number of PCB

8.4. Delivery accepted by the customers implies that he will not contest the conformity to the present Norm which were using his selected criteria for the tests, if made by the factory as per chapter 8.3 above. Customer can re-check by himself before acceptance.
Delivery acceptance by the customer does not wave the right to claim for a non-conformity to this Norm if the non-conformity cannot be detected before delivery and is discovered later, for example when using the boards.

8.5. This Norm recommends to establish a contract between the customer and the factory that indicates all testing and control procedures.

***

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APPENDIX A

TECHNICAL SHEET

CLIENT	MANUFACTURER	TECHNICAL SHEET (according to NF C 93-713)

RIGID PCB BOARD Nº								Index			
Single side ☐		Double Side ☐		Double Side ☐		Multilayer ☐					
NPTH				With PTH		Number of Layers ☐					
Punching ☐		Drilled ☐									
Dimension		Area		Class of the Board							
(mm x mm)		(dm²)		Flatness %							
Material Ref.:				Thickness (mm)							
NF C93-751 required ☐				Other Certificates required:							
Axes and origin indexing by:			Hole ☐		Targets for Optical aiming ☐						
The furthest hole from the original Distance L max (mm)											
Drawing Ref.:											
Routing		Drawing ☐		Program		Ref.:					
Holes	Positions	Grid & Map ☐		Drilling program ☐		Ref.:					
	According to	Reference side picture: ☐		Holes centers picture ☐		Ref.:					
	Quantity										
	Ø NPTH										
	Ø PTH										
	Ø VIA										
	Remarks										
Markings	Pictures ☐			Reference layer ☐		Ref.:					
	Program ☐			Verso ☐		Ref.:					
Solder Mask	On Bare Copper ☐			Pictures ☐		Reference layer ☐		Ref.:			
	On Oxidized Copper ☐			Program ☐		Verso ☐		Ref.:			
Coating	On Tin Lead ☐										
Chemical Gold	Standard ☐			Reference layer ☐		Ref.:					
	Other ☐			Verso ☐		Ref.:					
OSP finish	☐										
Tin Lead	Electro deposit ☐			Reference layer ☐		Ref.:					
	Refused ☐			Verso ☐		Ref.:					
	By rollers ☐										
	Hot Levelling ☐										
	Thick (100 µm) ☐										
Gravure Layer	Pictures ☐			Reference layer ☐		Ref.:					

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Customer's general specification ref :					
Additional requirement :					
Applies to:				**Additional :**	
Inserted components ☐	SMT ☐	Mix ☐		Thermal drain	☐
Components on	1 side ☐	2 sides ☐		Carbon ink	☐
Assembling	manual ☐	Automated ☐		Waved layers	☐
ZIF ☐				Other	☐

Multilayer PCB						
	Layer n#	**Copper thickness**	**Class**	**Reference**	**Prepreg thickness**	**Remark**
Reference	1					
				Total Thickness :		

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Appendix B

Multilayer PCB – class definition

Minimum difference between diameters (CAD values in mm)		Class					
		1	2	3	4	5	6(1)
Of a component pad and finished hole :	C ≤ 300 300<C≤460 460<C≤600			0,68 0,73 0,78	0,58 0,66 0,68	0,47 0,52 0,57	0,44 0,49 0,54
Of a via and the drilled hole :	C ≤ 300 300<C≤460 460<C≤600			0,53 0,58 0,63	0,43 0,48 0,53	0,32 0,37 0,42	0,29 0,34 0,39
Of a window (around a component hole) and a finished hole:	C ≤ 300 300<C≤460 460<C≤600			1,30 1,35 1,40	1,00 1,05 1,10	0,77 0,82 0,87	0,68 0,73 0,78
Of a window (around a component hole) and a drilled hole:	C ≤ 300 300<C≤460 460<C≤600			1,15 1,20 1,25	0,85 0,90 0,95	0,62 0,67 0,72	0,53 0,58 0,63
(1) Class 6 is just for reference C = long side of the board							

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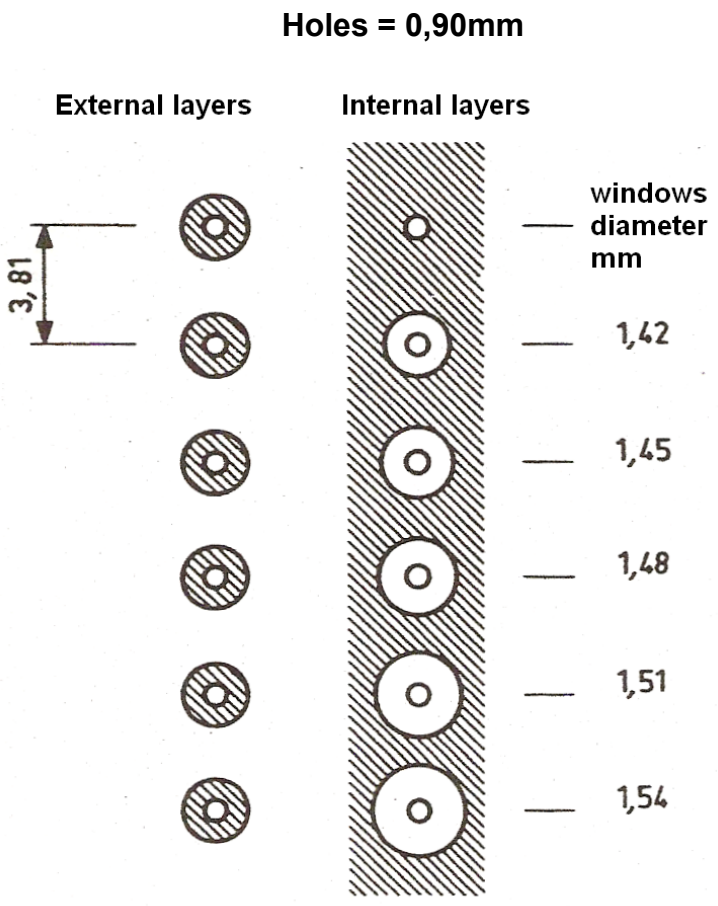
ANNEX C

INNER LAYERS MILSALIGNMENT

Method and principles
We use a test coupon (see chapter 5) similar to below sample with several plated holes. The holes diameters must be the most significant diameters used on the main PCB.
Holes are not connected to inner layers but go through them through “windows”.
Windows diameter is equal to the smallest pad size of each hole diameter.
During electric test, short cut between pads and inner layers will show that misalignment is too important at this place and exceeding the acceptable limit.
Additional holes and windows, with diameters lower than those required for the board can help evaluate misalignment values.
This measurement can be used to know what happen next to the test coupons on the board, and it can be useful to put several test coupons around the board.

INFORMATION GATHERED THROUGH THIS METHOD IS ONLY STATISTICAL : IT IS USEFUL TO GET AN IDEA ON THE MASS PRODUCTION QUALITY BUT CANNOT BE USED TO JUDGE EACH BOARD.

Example : Class 4 ; C=300; holes=0,90mm ; inner layer pad = 1,48mm



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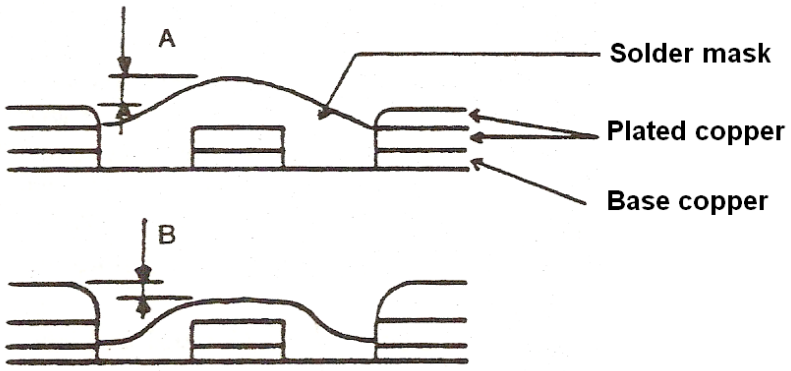
ANNEX D

SOLDER MASK THICKNESS REQUIREMENT



Acceptable values for A or B are to be agreed between customer and manufacturer. They depend on solder mask and SMT technologies used for assembly.

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ANNEX E

SOLDER MASK LAYOUT REQUIREMENT

Misalignment between solder mask and copper is acceptable within below limits.

a) Minimal distance between solder mask opening and hole edge :

Tolerance (see fig. E1) :
d ≥0,05mm for plated holes
d ≥0,1mm for non plated holes with HAL finished pad
d ≥0,2mm for non plated holes with copper pad.

Solder mask on pad(for SMC)
Tolerance : d≤0,2mm (see fig E1 bis) outside landing zone Z (see chapter 1.4.3)

b) maximum uncovered area on the edge and on the wall of a copper line near a hole (see fig. E2)
Tolerance : d≤0,05mm (see fig E2)

c) maximum size of uncovered area on the edge and on the wall of a copper line (see fig. E3)
Tolerance : d≤0,05mm and L≤1mm

d) maximum length of uncovered area on the wall only of a copper line (shadow).
Uncovered area facing another (see fig E4):
Tolerance : L≤4mm

Uncovered area on one side only (see fig E5) :
Tolerance : L≤4mm

e) solder mask missing between two pads without line (see fig E6)
Tolerance : L≤1mm

f) solder mask on pads with no hole for testing points :
Tolerance : tolerated on less than 50% of the pad area

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ANNEX F

VISUAL EXAMINATION GUIDE

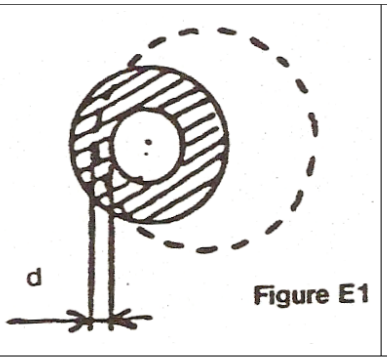

Figure E1

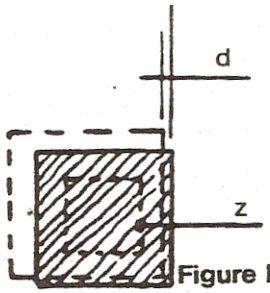

Figure E1 bis

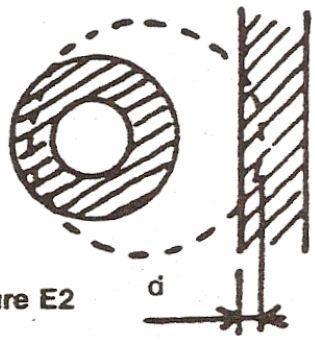

Figure E2

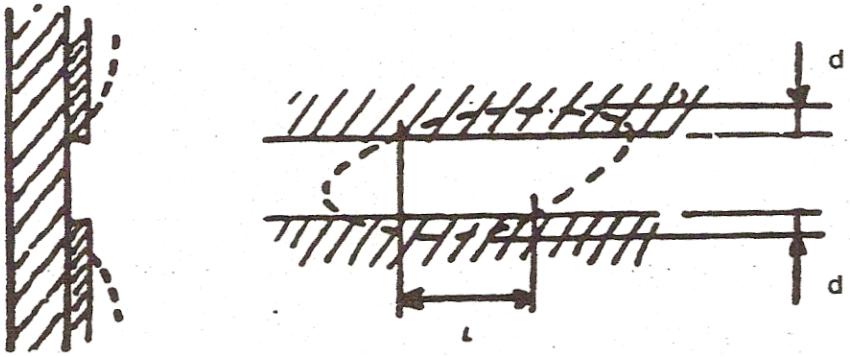

Figure E3

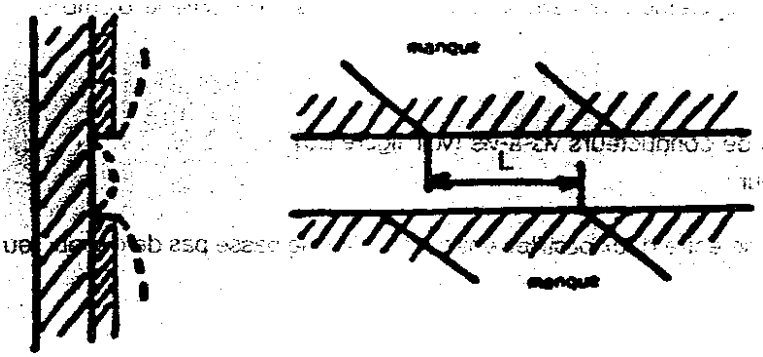

Figure E4

Figure E5

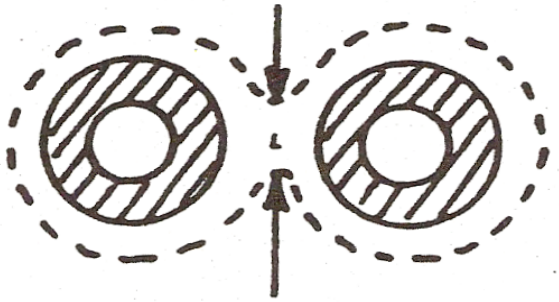

Figure E6

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ANNEX F

VISUAL EXAMINATION GUIDE
HOW TO DETERMINE VISUAL DEFAULTS

(Visual examination is conducted under normal lighting with a 10x magnifier fitted with a 50um scale.

Below listed defaults are indicated as Major (M), minor (m) or Great (G).
NFC93-721 “repairs of bare PCB” norm and UTEC93-723 guide must also be taken into consideration.

F1. Routing

- Mistakes in slots and/or outside routing	M
- Copper	G
- Small non recurrent mistakes	m
Or if more than one mistakes every 100mm	G

F2. Drilling

F2.1.Drilling defaults

- filled hole, additional	M
filled hole, missing	G
- Hole edge damaged:	
If the hole is intended to hold the board:	
Impossible to hold the board	M
Possible to hold the board	G
- Edges blur, uneven holes or slot , can be seen without magnifier	m
- Holes diameter out of tolerances except if smaller than requested for plated holes	M

F2.2.Holes Plating defaults

- Missing plating	M
Or plating when not necessary, or not important	G or M
- Defaults in plating:	
- pulled away, with excessive burr or plugging the hole	M
- void or microvoid of more than 10% of the plated area	M
- void or microvoid of less than 10% of the plated area can be accepted if they do not occur on both sides of the hole	m

F3. Copper stripping

F3.1.General requirements

- line or pad missing totally or partially, cut or short cut	M
- Copper stripping or with possible stripping because of defaults such as copper and laminate damaged, bubbles, waves undercut , outgrow, overhang that can be seen without magnifier	M
- Corrosion	M
- Oxidation	G
- Defaults in HAL over 5% of area	G
- edge roughness, nicks, pinholes etc. that can be seen without magnifier:	
Locally	m
On the whole board	M

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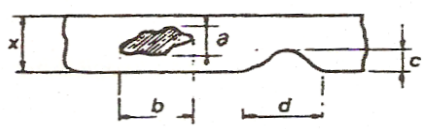
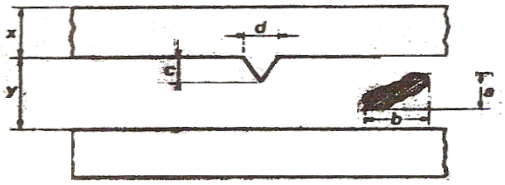
F3.2.Lines

- Lines damage, nicks, pinholes etc. that will reduce over 30% of copper thickness:
  On whole length M
  Same default on half or more of the width G
- Scratch or damage on solder mask that will show copper on the whole length M
  Same default on half or more of the width G
- Random defaults such as edge roughness, nicks, pinholes etc. that can reduce width below minimal value and above below tolerance: M

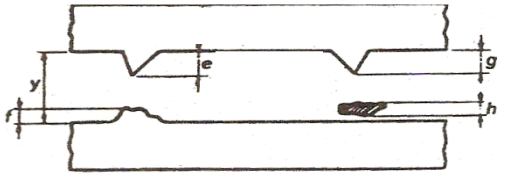


a ⩽ 20 % of x,
b ⩽ x,
c ⩽ 20 % of x,
d ⩽ x,
x : line width

- Lines damage, nicks, pinholes etc. that will reduce over 30% of copper thickness:
  On whole length M
  Same default on half or more of the width G
- Scratch or damage on solder mask that will show copper on the whole length M



c ≤ 20% of y,
a ≤ 20% of y,
d ≤ x,
b ≤ y and ≤ 2mm.



(e+f) ≤ 20% of y,
(g+h) ≤ 20% of y.

F3.3.Pads

- Pads damages like nicks, pinholes etc. :
  that will reduce copper around the hole below value from the class M
  That will reduce copper adhesion on substrate M
- Tolerance per pad : one scratch of less than 0,25mm m

F3.4.Large copper areas

- Area damages like nicks, pinholes etc. :
  In the components zone M
- That will reduce copper adhesion on substrate M

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F3.5.Large copper areas

F3.5.1. Definition

Line edges capability can be defined by the distance between maximal and minimum width of the line.
For linear edges, distance between minimum and maximum line width is measured in 10mm sections (fig.F.3.5.1).
For curved lines :

- if curve diameter is ≥ 20mm the distance between minimum and maximum line width is measured on a 10mm arc (fig F.3.5.2)
- if curve diameter is < 20mm the distance between minimum and maximum line width is measured :
  - on a length equal to the arc length if change of direction is < 90 deg.
  - on a length equal to a 90 deg arc if change of direction is > 90 deg. (fig F.3.5.3)

F3.5.2. Tolerance

Distance between minimum and maximum line width must be lower than copper thickness.

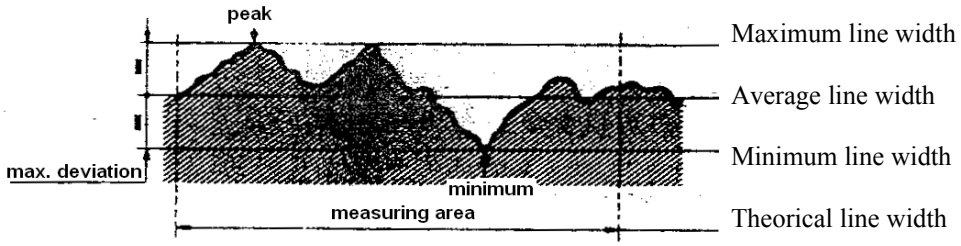

Fig.F3.5.1

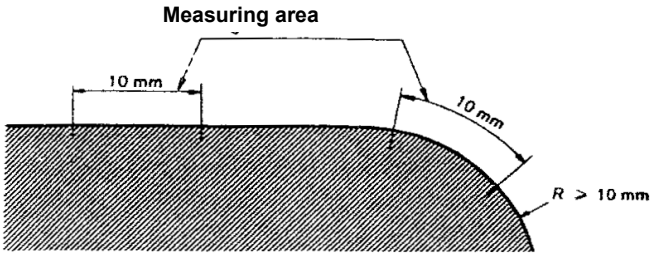

Fig.F3.5.2

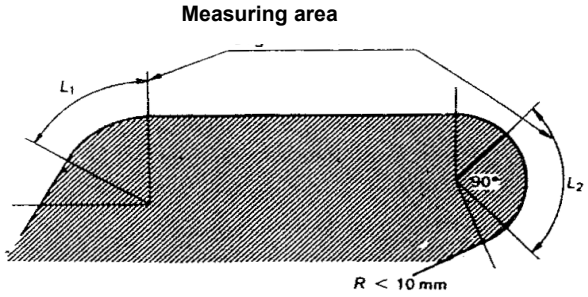

Fig.F3.5.3

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F3.6.Contact area

On the contact area as defined in the technical specification :

- Any default up to the laminate :	M
- We can tolerate one pit per contact area and 3 pits maximum per board	m

Outside the contact area, including on the lines within 3mm distance from the contact area :

- Any damage, nicks, pinholes,cracks :	G
- Pits, grains, scratches	m

F4. Isolating material

- Missing chamfering or damage to chamfering	G
- Missing homogenous aspect	m
- Foreign particle inclusion (seen without magnifier)	M
- Delamination on a double side board	G
Delamination on a multi layer board	M
- Local measling	m
- Measling on the whole board	M

F5. Solder mask

The general aspect of the board must be homogeneous and must not show bubbles or pits. It is tolerated to have a cloth aspect for silk screen deposed solder mask.
The copper must never be seen throught pits, scratches or damages in the solder mask.
The area covered by the solder mask must be those specified in the technical files.

Local missing and excess of solder mask are tolerated if :

- Missing area is in an area without lines
- Solder mask drops are small and outside conductive areas and areas with mechanical function (connectors, sliding parts etc) as indicated in the technical files;
- Local solder mask drops in holes other than holes for components and for locating;
- Solder mask drips in vias;

- bubbles	G
- Pits with solder mask lifting	M
- Non-homogenous color	G
- Missing solder mask when needed on the drawing	G
- Solder mask drops on area with no electrical or mecanical function	m
- Solder mask on area where it was not requested in the files	G
- Solder mask drippings in plated holes for components	M

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ANNEX G

GUIDE FOR ACCEPTING DELIVERY OF PCB AND TO SOLVE LITIGATION

Acceptation of a delivery by the Customer must be done , or is implied within an agreed period of time.
In case of rejection of the delivery, the customer must :

1. inform the manufacturer and indicate the reason for rejectin the delivery ;
2. If manufacturer requires, another visual and contradictory inspection of the litigated delivery must be done in the customer's premises ;
3. If the customer accepts, manufacturer can sort out the delivery to submit part of the delivery to customer's acceptance
4. defective boards are returned to the manufacturer after sorting.

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ANNEX H

GUIDE TO EXPLAIN THE CLASSES WHICH CORRESPOND TO MINIMUM DIMENSONS OR TOLERANCE ON A CIRCUIT.

This table includes some key up to class 6. The class 6 is given as project only.

Mini values of conception	1	2	3	4	5	6
Mini-width of conductors	0,8	0,5	0,31	0,21	0,15	0,12
Mini space between conductors	0,68	0,5	0,31	0,21	0,15	0,12
Mini Space diam. Past/TNM	1,57	1,13	0,90			
Mini Space diam. Past/TM	1,19	0,78	0,60	0,49	0,39	0,35
Mini-Space via past/ through holes		0,45	0,34	0,24	0,20	
Tolerances on finished card*	1	2	3	4	5	6
Width and space of conductive parts (+ or -)	0,24	0,15	0,08	0,06	0,05	0,04
** regards to conception values or supplied documents*						
Mini-values on finished card	1	2	3	4	5	6
Mini width** of conductors	0,46	0,30	0,20	0,13	0,08	0,05
Mini-space between conductive parts.	0,36	0,30	0,20	0,13	0,08	0,05
*** Values found thanks to mini limit value of the doc if these are support.*						
Internal layers						
Mini-distance between the conductive window and the non-connected through hole wall		0,33	0,23	0,17	0,14	
Clearance VEB/past/plage	0,34	0,25	0,15	0,10	0,07	0,06
Mini-line of SOM	0,80	0,50	0,31	0,21	0,15	0,12
**** SOM= Solder Mask*						

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